## We claim:

| 1 | 1. | An apparatus, comprising:  |
|---|----|--|
| 2 |    | an integrated circuit including  |
| 3 |    | a first processor with a first dedicated cache;  |
| 4 |    | a second processor with a second dedicated cache; and                                    |
| 5 |    | control logic coupled to the first and second dedicated caches to transfer               |
| 6 |    | first data from the first dedicated cache to the second dedicated                        |
| 7 |    | cache entirely within the integrated circuit.  |
|   |    |  |
| 1 | 2. | The apparatus of claim 1, wherein:   |
| 2 |    | the control logic is to transfer the first data if the first data is a cache line in the |
| 3 |    | first dedicated cache and not in the second dedicated cache.                             |
|   |    |  |
| 1 | 3. | The apparatus of claim 1, wherein:   |
| 2 |    | the control logic is to transfer the first data if the first data is a modified version  |
| 3 |    | of a particular cache line and the second dedicated cache contains an                    |
| 4 |    | unmodified version of the particular cache line.   |
|   |    |  |
| 1 | 4. | The apparatus of claim 1, further comprising:  |
| 2 |    | a coherency unit to perform snoop operations on the first and second dedicated           |
| 3 |    | caches.  |

| 1   | <i>5.</i> | The apparatus of claim 1, wherein:  |
|-----|-----------|---|
| 2   |           | the control logic is further to transfer second data from the second dedicated    |
| . 3 |           | cache to the first dedicated cache entirely within the integrated circuit.        |
|     |           |   |
| 1   | 6.        | The apparatus of claim 1, wherein the integrated circuit further includes:        |
| 2   |           | a shared cache coupled to the control logic and to the second dedicated cache to  |
| 3   |           | provide the first data to the second dedicated cache;                             |
| 4   |           | wherein the control logic includes a write buffer to receive the first data from  |
| 5   |           | the first dedicated cache and to provide the first data to the shared cache       |
|     |           |   |
| 1   | 7.        | The apparatus of claim 1, wherein the integrated circuit further includes:        |
| 2   |           | a shared cache coupled to the control logic, to the first dedicated cache, and to |
| 3   |           | the second dedicated cache;   |
| 4   |           | wherein the control logic is further to transfer second data from the second      |
| 5   |           | dedicated cache to the first dedicated cache;                                     |
| 6   |           | wherein the control logic includes a first write buffer to receive the first data |
| 7   |           | from the first dedicated cache and to provide the first data to the shared        |
| 8   |           | cache, and further includes a second write buffer to receive the second           |
| 9   |           | data from the second dedicated cache and provide the second data to the           |
| 10  |           | shared cache;   |
| 11  |           | wherein the shared cache is to provide the first data to the second dedicated     |
| 12  |           | cache and to provide the second data to the first dedicated cache.                |

| 1  | 8.  | The apparatus of claim 1, wherein:   |
|----|-----|--|
| 2  |     | the control logic includes a fill buffer coupled to first and second dedicated       |
| 3  |     | caches to receive the first data from the first dedicated cache and to               |
| 4  |     | provide the first data to the second dedicated cache.                                |
|    |     |  |
| 1  | 9.  | The apparatus of claim 1, wherein:   |
| 2  |     | the control logic includes a first fill buffer coupled to the first and second       |
| 3  |     | dedicated caches to receive the first data from the first dedicated cache            |
| 4  |     | and to provide the first data to the second dedicated cache; and                     |
| 5  |     | the control logic includes a second fill buffer coupled to the first and second      |
| 6  |     | dedicated caches to receive second data from the second dedicated cache              |
| 7  |     | and to provide the second data to the first dedicated cache                          |
|    |     |  |
| 1  | 10. | The apparatus of claim 1, wherein the control logic includes:                        |
| 2  |     | a multiplexer coupled to the first and second caches to receive the first data       |
| 3  |     | from the first dedicated cache and to provide the first data to the second           |
| 4  |     | dedicated cache.   |
|    |     |  |
| 1. | 11. | The apparatus of claim 1, wherein the control logic includes:                        |
| 2  |     | a first multiplexer coupled to the first and second caches to receive the first data |
| 3  |     | from the first dedicated cache and to provide the first data to the second           |
| 4  |     | dedicated cache; and   |
| 5  |     | a second multiplexer coupled to the first and second caches to receive second        |
| 6  |     | data from the second dedicated cache and to provide the second data to               |
|    |     |  |

the first dedicated cache.

| 1 | 12. | A method, comprising:  |
|---|-----|--|
| 2 |     | transferring first data from a first dedicated cache of a chip multi-processor to      |
| 3 |     | control logic in the chip multi-processor, entirely within the chip multi-             |
| 4 |     | processor; and   |
| 5 |     | subsequently transferring the first data from the control logic to a second            |
| 6 |     | dedicated cache of the chip multi-processor, entirely within the chip                  |
| 7 | *   | multi-processor.   |
|   |     |  |
| 1 | 13. | The method of claim 12, further comprising:  |
| 2 |     | transferring second data from the second dedicated cache to the control logic,         |
| 3 |     | entirely within the chip multi-processor; and  |
| 4 |     | subsequently transferring the second data from the control logic to the first          |
| 5 |     | dedicated cache, entirely within the chip multi-processor.                             |
|   |     |  |
| 1 | 14. | The method of claim 12, wherein:   |
| 2 |     | the transferring the first data from the first dedicated cache includes transferring   |
| 3 |     | the first data from the first dedicated cache to a write buffer;                       |
| 4 |     | the transferring the first data from the control logic includes transferring the first |
| 5 |     | data from the write buffer to a shared cache.  |
|   |     | <b>.</b>   |
| 1 | 15. | The method of claim 14, wherein:   |
| 2 |     | the transferring the first data from the control logic further includes transferring   |
| 3 |     | the first data from the shared cache to the second dedicated cache.                    |

| 1  | 16. | The method of claim 12, wherein:   |
|----|-----|--|
| 2  |     | the transferring the first data from the first dedicated cache includes transferring   |
| 3  |     | the first data from the first dedicated cache to a fill buffer;                        |
| 4  |     | the transferring the first data from the control logic includes transferring the first |
| 5  |     | data from the fill buffer to the second dedicated cache.                               |
|    |     |  |
| 1  | 17. | The method of claim 12, wherein:   |
| 2  |     | the transferring the first data from the first dedicated cache includes transferring   |
| 3  |     | the first data from the first dedicated cache to a multiplexer; and                    |
| 4  |     | the transferring the first data from the control logic includes transferring the first |
| 5  |     | data from the multiplexer to the second dedicated cache.                               |
|    |     |  |
| 1  | 18. | A system, comprising:  |
| 2  |     | a main memory,   |
| 3  |     | a chip multiprocessor coupled to the main memory and including:                        |
| 4  |     | a first processor with a first dedicated cache;  |
| 5. |     | a second processor with a second dedicated cache; and                                  |
| 6  |     | control logic coupled to the first and second dedicated caches to transfer             |
| 7  |     | first data from the first dedicated cache to the second dedicated                      |
| 8  |     | cache entirely within the chip multiprocessor.   |

| 1  | 19.         | The system of claim 18, wherein:   |
|----|-------------|--|
| 2  |             | the control logic is further to transfer second data from the second             |
| 3  |             | dedicated cache to the first dedicated cache entirely within the                 |
| 4  |             | chip multiprocessor.   |
|    |             |  |
| 1  | 20.         | The system of claim 18, wherein the chip multiprocessor further includes:        |
| 2  |             | a shared cache coupled to the control logic and to the second dedicated cache to |
| 3  |             | provide the first data to the second dedicated cache;                            |
| 4  |             | wherein the control logic includes a write buffer to receive the first data from |
| 5  |             | the first dedicated cache and to provide the first data to the shared cache      |
|    |             |  |
| 1  | 21.         | The system of claim 18, wherein:   |
| 2  | •           | the control logic includes a fill buffer coupled to first and second dedicated   |
| 3  |             | caches to receive the first data from the first dedicated cache and to           |
| 4  |             | provide the first data to the second dedicated cache.                            |
|    |             |  |
| 1  | 22.         | The system of claim 18, wherein the control logic includes:                      |
| 2. |             | a multiplexer coupled to the first and second dedicated caches to receive the    |
| 3  |             | first data from the first dedicated cache and to provide the first data to       |
| 4  |             | the second dedicated cache.  |
|    |             |  |
| 1  | 23.         | A machine-readable medium that provides instructions, which when executed        |
| 2  | by a s      | et of one or more processors, cause said set of processors to perform operations |
| 3  | comprising: |  |

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|---|-----|--|
| 4 |     | transferring data from a first dedicated cache in an integrated circuit to control |
| 5 |     | logic in the integrated circuit, entirely within the integrated circuit; and       |
| 6 |     | subsequently transferring the data from the control logic to a second dedicated    |
| 7 |     | cache of the integrated circuit, entirely within the integrated circuit.           |
| 1 | 24. | The medium of claim 23, wherein:   |
|   |     |  |
| 2 |     | the transferring the data from the first dedicated cache includes transferring the |
| 3 |     | data from the first dedicated cache to a write buffer; and                         |
| 4 |     | the transferring the data from the control logic includes transferring the data    |
| 5 |     | from the write buffer to a shared cache and subsequently transferring the          |
| 6 |     | data from the shared cache to the second dedicated cache.                          |
| 1 | 25. | The medium of claim 23, wherein:   |
| 2 | -   | the transferring the data from the first dedicated cache includes transferring the |
| 3 |     | data from the first dedicated cache to a fill buffer; and                          |
| 4 |     | the transferring the data from the control logic includes transferring the data    |
| 5 |     | from the fill buffer to the second dedicated cache.                                |
|   |     |  |
| 1 | 26. | The medium of claim 23, wherein:   |
| 2 |     | the transferring the data from the first dedicated cache includes transferring the |
| 3 |     | data from the first dedicated cache to a multiplexer; and                          |
| 4 |     | the transferring the data from the control logic includes transferring the data    |

from the multiplexer to the second dedicated cache.